6. (Original) The system of claim 5 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences.

7. (Original) The system of claim 6:

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise sixteen Hadamard sequences selected as every sixteenth sequence in the defined order.

8. (Original) The system of claim 4 wherein the second sequence consists of sixteen of the code words.

9. (Original) The system of claim 8 wherein the plurality of Hadamard sequences are selected from a set of 256 Walsh sequences.

10. (Original) The system of claim 6:

wherein the 256 Walsh sequences have a defined order; and

wherein the plurality of Hadamard sequences comprise seventeen Hadamard sequences selected as every eighth sequence in the defined order.

11. (Previously amended) The system of claim 1 wherein the circuit for providing the secondary synchronization code comprises:

a circuit for performing an exclusive OR operation between the second sequence and the third sequence; and

a circuit for providing the secondary synchronization code in response to the exclusive OR operation.

12. (Original) The system of claim 1:

wherein the primary synchronization code comprises 8-bit values A and B and complements of the values A and B;

wherein the value A comprises a sequence A = { 1, 1, 1, 1, 1, 1, -1, -1 };

wherein the value B comprises a sequence B = { 1, -1, 1, -1, 1, -1, -1, 1 }; and

wherein the primary synchronization code comprises a 256-bit sequence {A, B, A, B, A, B, -A, -B, -A, -B, A, B, -A, -B, -A, -B, A, B, A, B, A, B, -A, -B, A, B, -A, -B, A, B, A, B}.

13. (Original) The system of claim 12:

wherein the second sequence comprises 256 bits; and

wherein the third sequence comprises 32 repeated instances of the value A.

14. (Previously amended) The system of claim 13 wherein the circuit for providing the secondary synchronization code comprises:

a circuit for performing an exclusive OR operation between the second sequence and the third sequence; and

a circuit for providing the secondary synchronization code in response to the exclusive OR operation.

15. (Original) The system of claim 14:

wherein the second sequence comprises a plurality of code words; and

wherein each of the plurality of code words is selected from a plurality of Hadamard sequences.

16. (Original) The system of claim 12:

wherein the second sequence comprises 256 bits;

wherein a complement of the value A is represented as -A; and

wherein the third sequence comprises a 256-bit sequence {-A, -A, -A, -A, A, -A, -A, A, -A, A, A, -A, -A, A, A, A, A, A, A, -A, -A, -A, A, A, -A, A, A, A, -A, A, -A, A, -A}.

17. (Previously amended) The system of claim 16 wherein the circuit for providing the secondary synchronization code comprises: